

CUSTOMER CASE STUDY

Thumbs up for low cost design tools

A limited budget need not restrict design aspirations as Dresden-based spin-off found with its first project, a high profile, complex, mixed signal IC chipset, delivered 'right first time, on time'.

Increasing demand for complex, mixed-signal IC designs prompted Stuttgart-based engineering company, Productivity Engineering, to expand the capability of its digital IC, gate array and FPGA design centre. But a severe shortage of the necessary analogue IC design skills in the area, forced it to consider another route. The result is PE-IC Design, now a two year old spin-off, based in Dresden, in Germany's Silicon Saxony. Run by Stefan Schubert, a veteran mixed signal IC designer, the fabless design house now employs five full time, experienced design engineers and a number of freelance contractors.

"A key advantage for PE-IC Design, as a spin-off, rather than a start-up, is that we kick-started with a number of substantial projects," Schubert explained. "The downside was, that as a design services company, we were unlikely to attract venture capital, and so purchasing design tools, for example, was an issue." PE-IC Design was on a tight schedule from Day 1. Its first major project, funded by the US National Institute of Justice, was for a three chip set, plus test chip, for a finger print recognition system application. Based on capacitive sensor signal conditioning technology, these mixed signal designs are complex.

The analogue multiplexer IC, for example, features two analogue inputs and 100 outputs, switches, control logic and output drivers. A shift register controls the analogue switches. Meanwhile, the 100 channel, 10bit capacitive sense IC contains all the amplification, rectification and data conversion circuitry necessary for synchronous evaluation of small AC currents in the 1 to 10MHz range. Current to voltage converters, amplifiers, synchronous rectifiers, L/P filters, 10bit ADC and data memory are implemented per input line, enabling parallel operation and scalability. Indeed, the overall design was engineered to be scalable on a daisy chain principle, allowing the creation of systems with virtually unlimited number of outputs. The result is that fingerprint recognition technology is easily scalable to palm print reading and recognition.

In addition, the system had to be fast – in fact, it delivers sensor data to the host in just 25ms, and power consumption had to be low – it is better than 100mA, and less if data acquisition speed is reduced.

Training not needed

Schubert's extensive design experience has mostly been with large companies using comprehensive, but expensive, Cadence tools. But a past partnership with a design subcontractor had brought the low cost Tanner EDA tools to his attention. "I'd seen these tools in action. They appeared to be 'grown-up' tools, and importantly,

they worked. We needed something immediately and it had to be affordable, so we decided to give it a try," Schubert recalled. The team started with several licences of the schematic capture and simulation tools, S-Edit and T-Spice, delivered and supported by Tanner's European distributor, EDA Solutions. Later, as the design progressed, PE-IC Design added the layout and verification software packages.

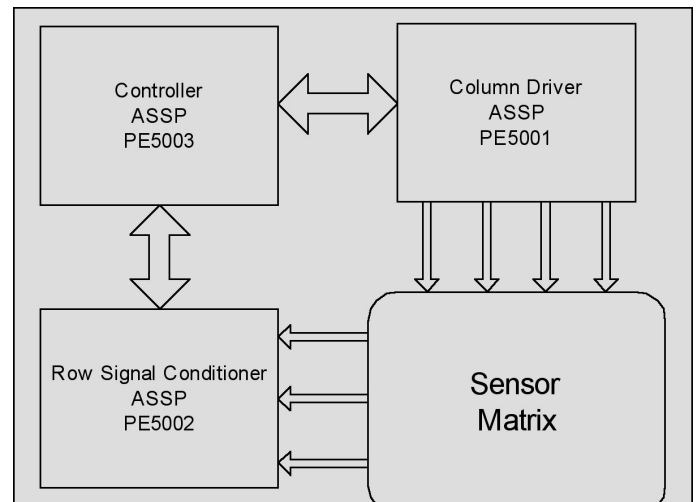


Diagram 1: The principle building blocks of PE-IC Design's capacitive sensor array. This Project was funded by the National Institute of Justice, Office of Justice Programs, US Department of Justice, project number 2005-IJ-CX-K067

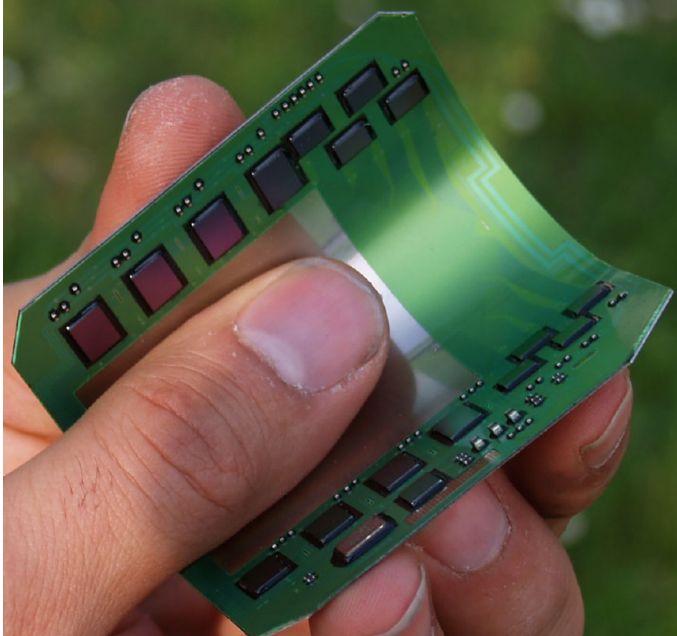
"There was some strong resistance from our most experienced engineers," Schubert said. "They were not initially, easily convinced that a Windows-based, low cost package would meet our requirements." But, the Tanner EDA tools swiftly proved to be up to the task. The software is supplied with comprehensive manuals and introductory tutorials. "The tools were intuitive to use and we had no problems getting under way," Schubert said.

Peter Kaiser of EDA Solutions commented: "Evidently the support material supplied is good, as they needed no training at all, and only needed to contact the UK support desk once or twice throughout the project."

With several engineers working on the chipset, the team was pleased to see the tools easily supported multi-user projects. "We were able to split up the design tasks allocating the various IC block designs to different engineers," Schubert added.

Simulation using the T-SpicePro package ran smoothly, once the models were available. The team had to work closely with the foundry, X-Fab, to produce the

quality of models needed for simulation. “The resulting simulation was a close reflection on the real end product,” Schubert confirmed. A slight limitation of the schematic tool, for faster abstraction and external scripting to create netlists, has already been addressed in the latest version of S-Edit.



PE-IC Design's capacitive sensor signal conditioning chip set, implemented on a flexible polymer substrate, will reduce the time to scan a fingerprint from 20s to just 1s

Two engineers were allocated to chip layout, using Tanner's L-Edit package. With no previous experience of these particular tools, the chip layout and verification processes also proceeded smoothly. Again, the engineers were impressed with the efficiency and functionality of the tools, particularly the interactive design rule checker (DRC) facilities, and the layout vs schematic (LVS) verification suite. They compared well with the more expensive tools they had previously used. The recent addition of 3D parasitic extraction features to Tanner's L-Edit chip layout tool will prove useful in future designs.

A final verification check, supporting some additional rules, was conducted by the foundry prior to tape-out. “But the cost of this extra verification service was far less than investing in expensive tools to do the job,” Schubert emphasised.

PE-IC Design is using Mentor Graphics tools for the digital design aspects not supported by the Tanner tools. But the company found it easy to integrate digital, analogue and mixed signal elements of the design later. Next, the company is investing in Mentor's high performance mixed signal simulator. “We need this

specialist capability from time to time, but the Tanner tools are well proven and used on a daily basis by all the team,” Schubert explained. The X-Fab foundry services are also used to place and route the digital circuitry, and the results can be integrated back to the Tanner tool suite.

From specification to tape-out took just nine months, and to final verification was 13 months, and the results were not only ‘right first time’ but also, on time. Final tweaks will reduce current consumption further and the design will move to production masks. This ‘right first time’ success is as much a function of the expertise of the design engineers as the capability and flexibility of the tool chain.

Helping hand

Meanwhile, the company is receiving considerable interest in the chipset, now available as a reference platform or demonstrator board. In finger print sensor applications, the chipset is implemented on a flexible polymer substrate. This has the potential of reducing the time taken to scan a print - down from 20s, using a conventional rigid substrate where the finger has to be rolled for a complete scan, to just 1s using the flexible approach based on PE's device.

Scaling up to a palm print sensor, a system might have 2500 x 4000 pixels, with a typical resolution from 500 to 800 pixels per inch, representing a 10million sensor array.

Other applications include use in hand prostheses and for patients with loss of sensory nerve function, to provide data on grip strength and to adjust motion control. Similarly, the devices might be used in haptics systems for adding a sense of touch to virtual reality applications.

Finally, a capacitive sensor array signal conditioning system can be used for monitoring liquid flow, with applications in industrial, environmental, food processing and medical industries.

Future developments

In addition to working concurrently on a number of digital IC design projects for its parent company, PE-IC Design is in discussion with external clients on another large mixed signal asic project, currently at the specification stage. The company will need to take on more engineers, and therefore more design tool licences as the business grows. Meanwhile, the PE-IC Design team is working closely with Tanner's software developers to provide feedback for next generation tool enhancements.

For further information, go to: www.pe-icdesign.de.